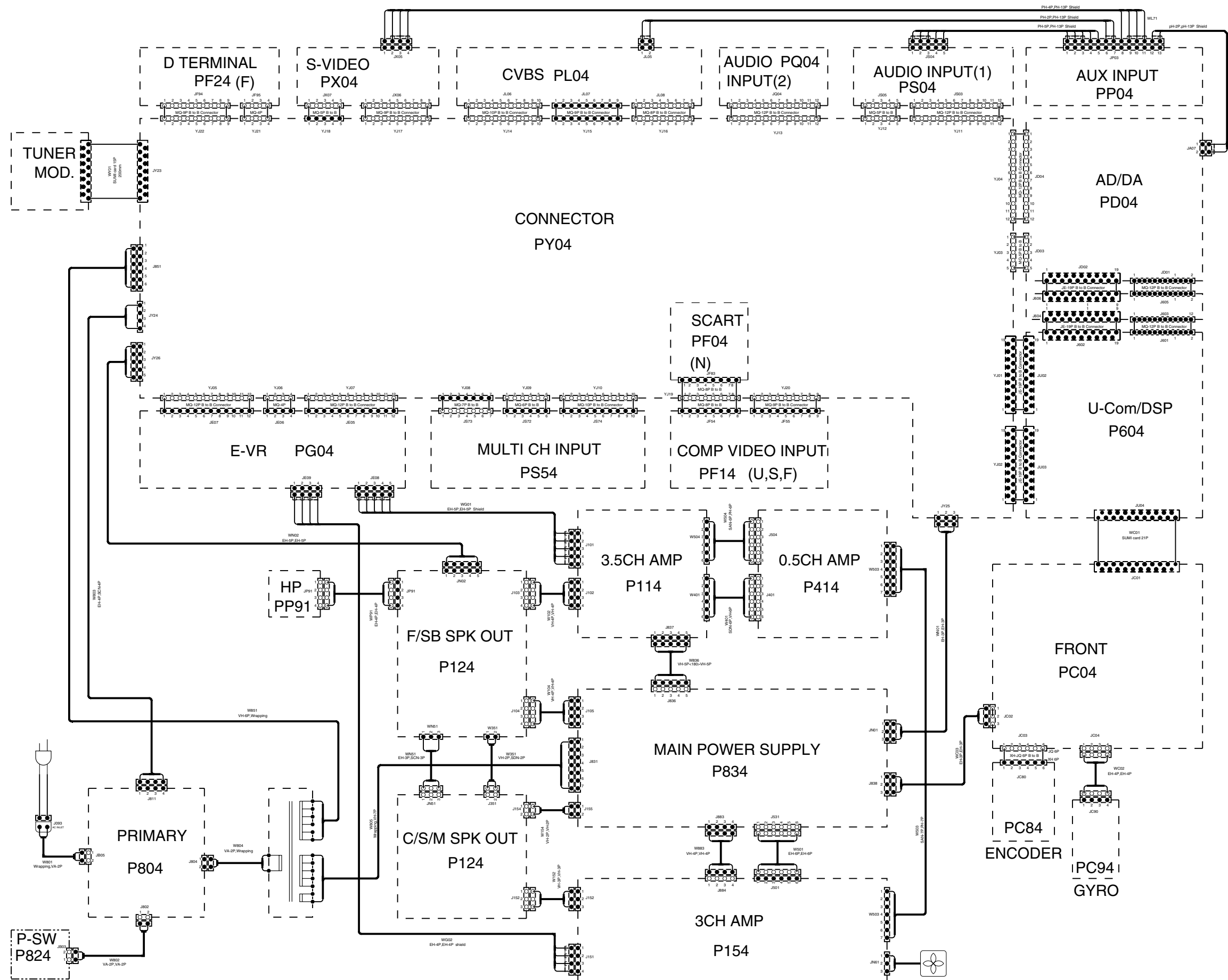
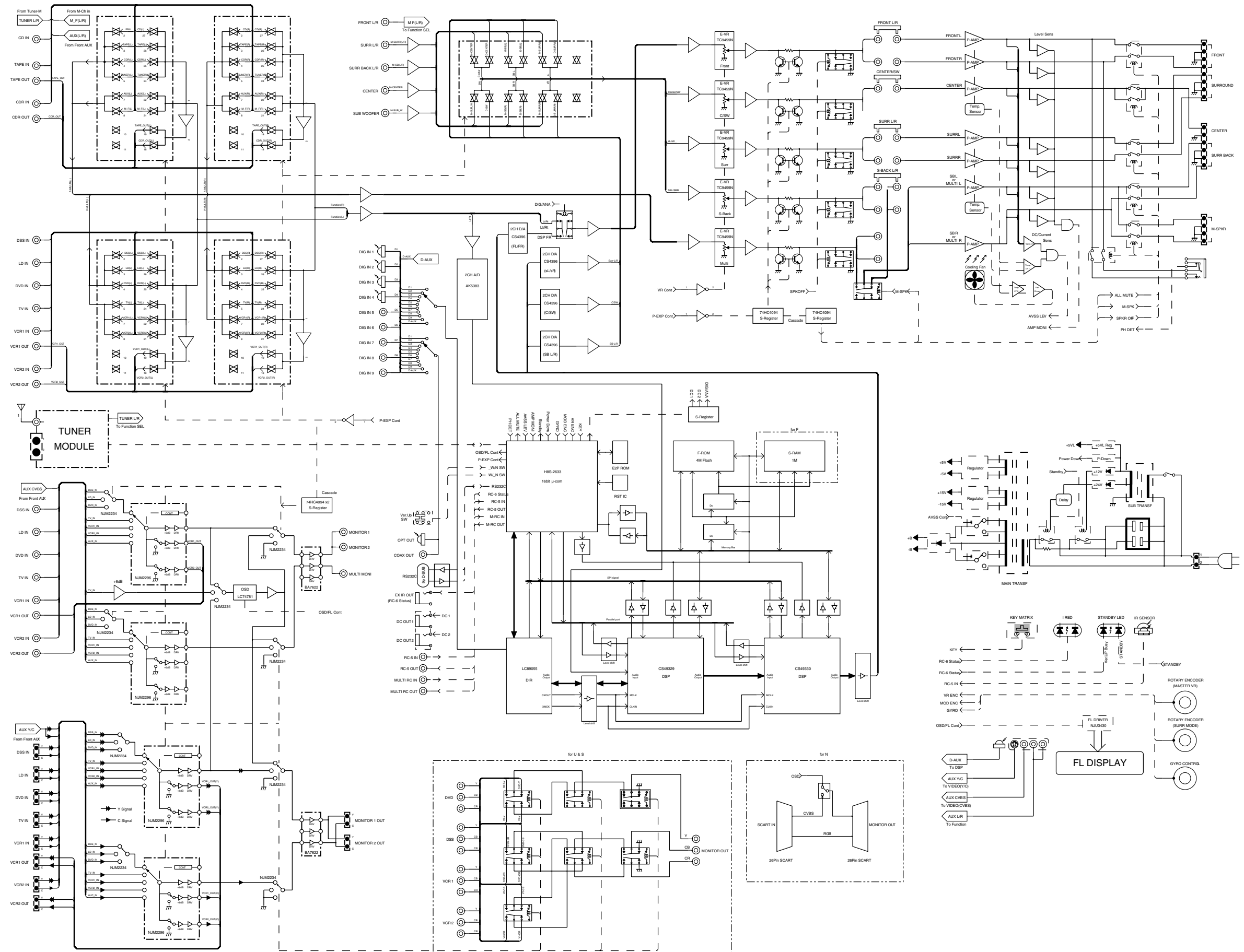


2. WIRING DIAGRAM

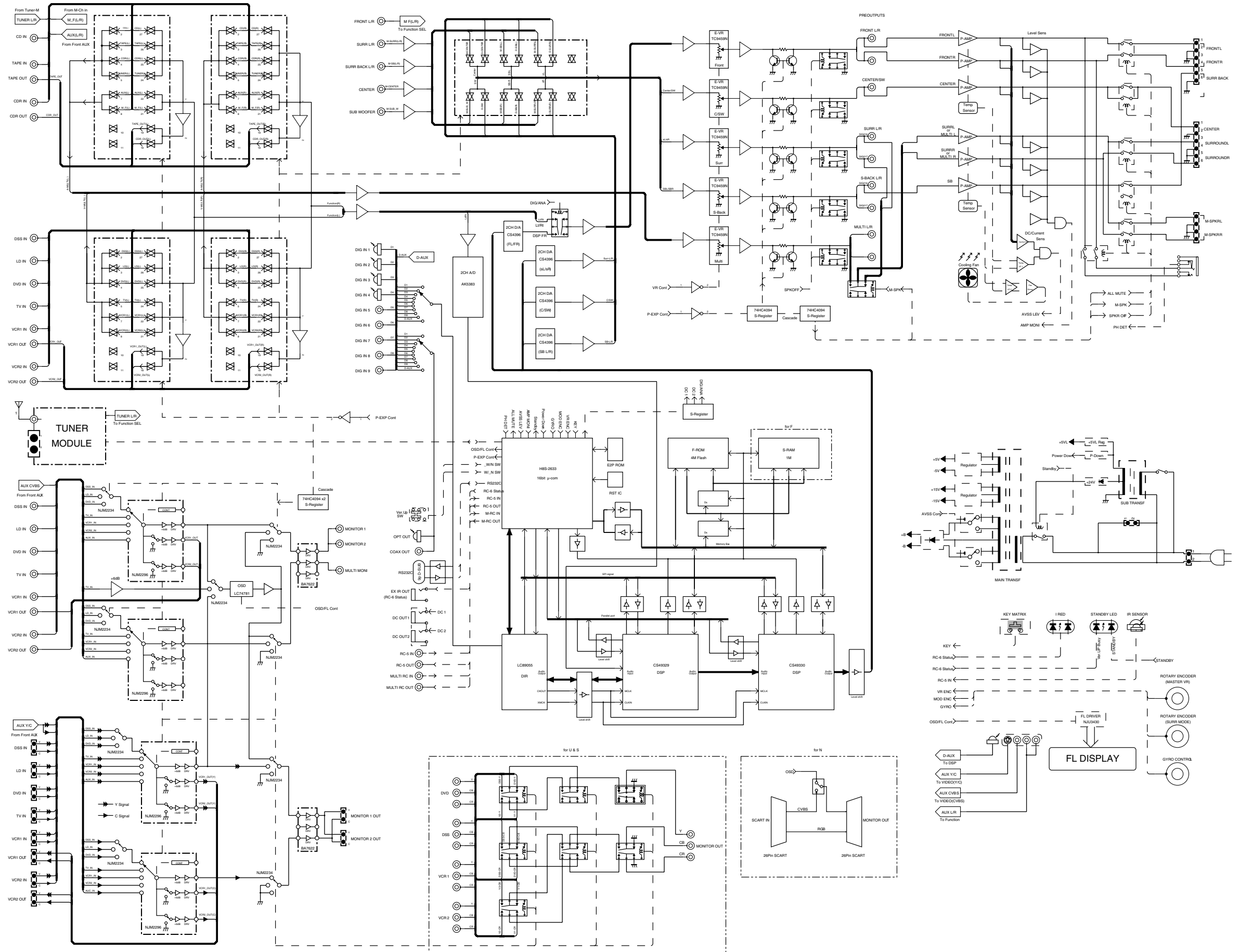


3. BLOCK DIAGRAM

SR9200 / PS9200

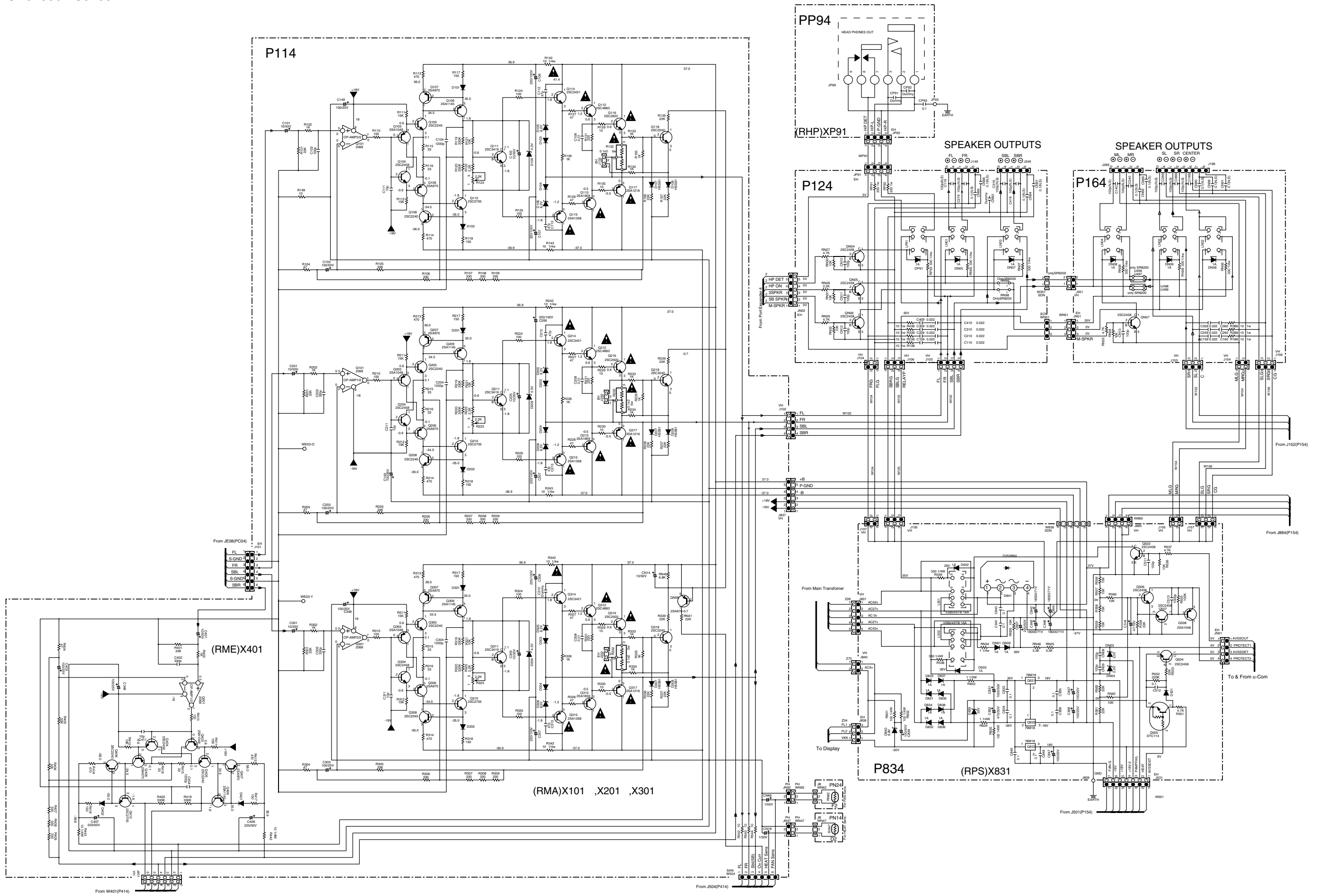


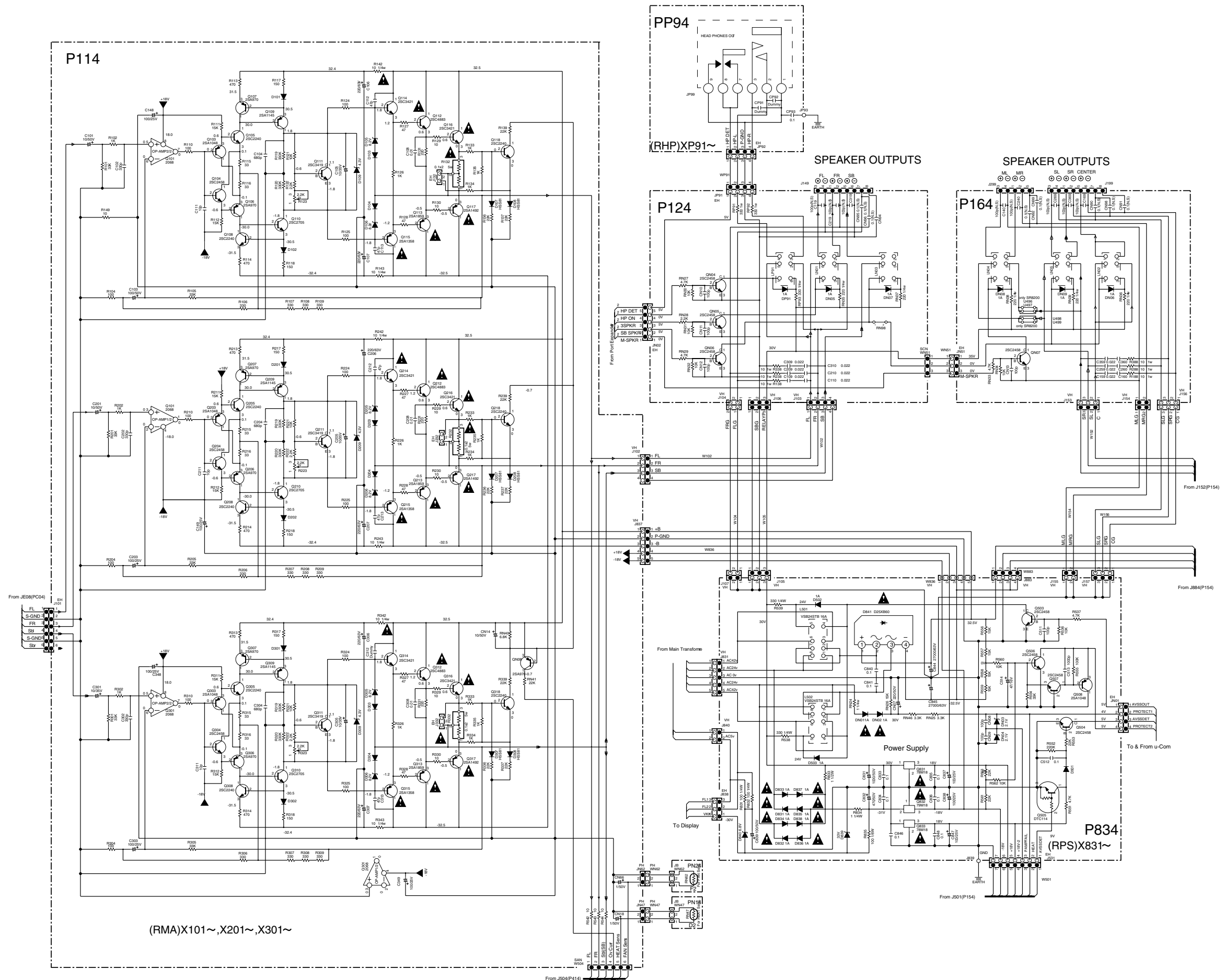
SR8200

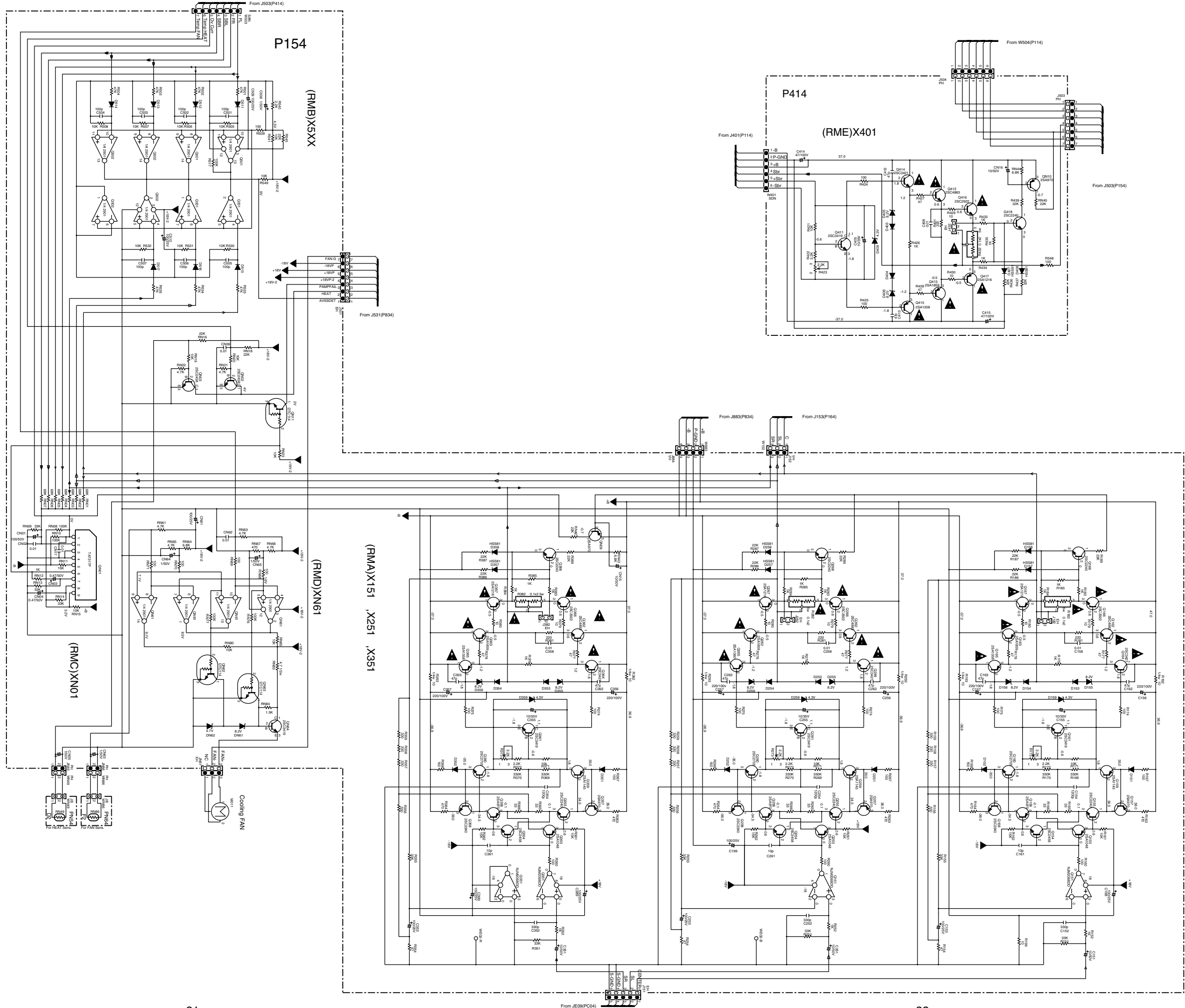


4. SCHEMATIC DIAGRAM

SR9200 / PS9200

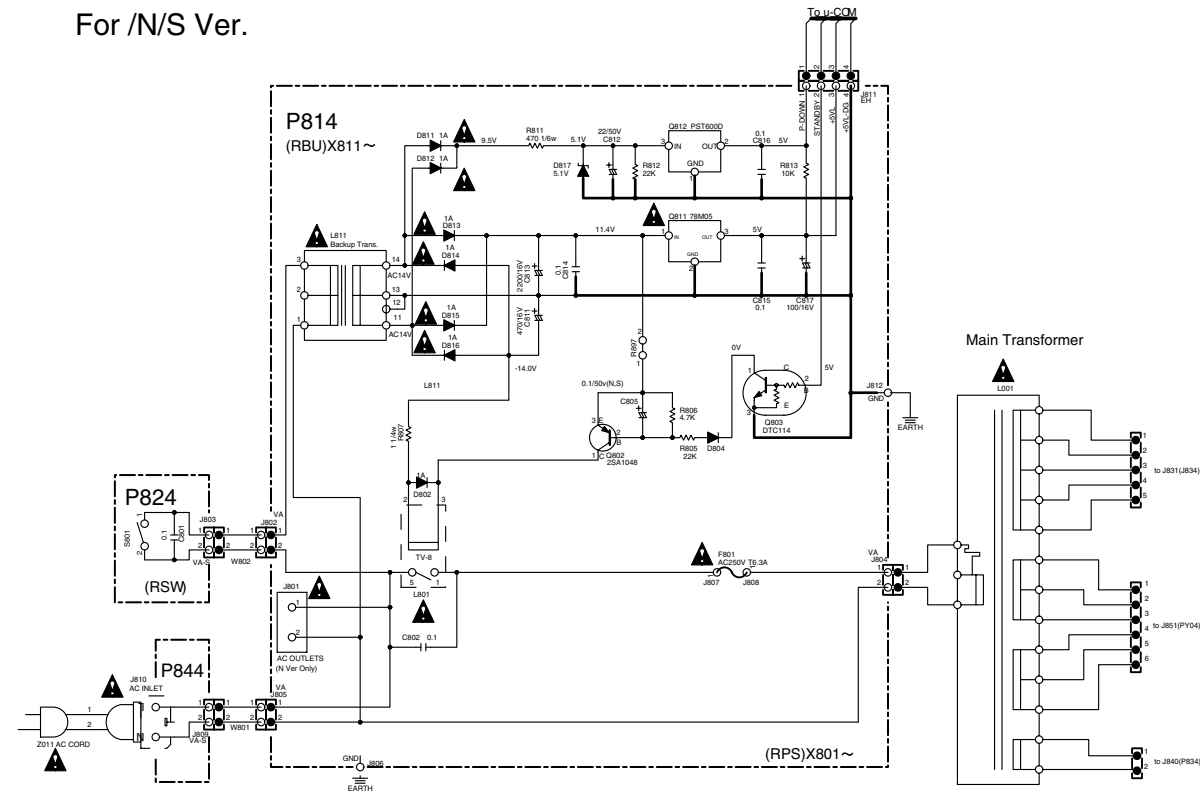




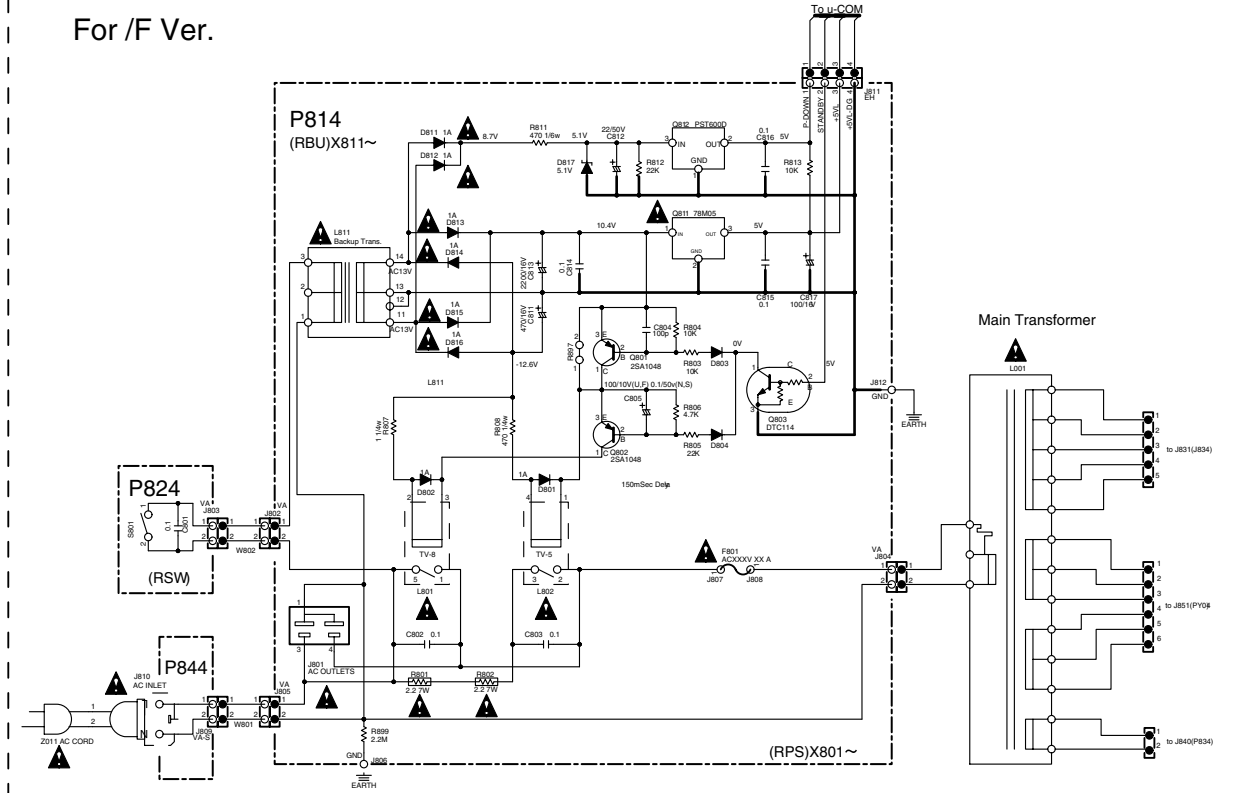


SR9200 / PS9200

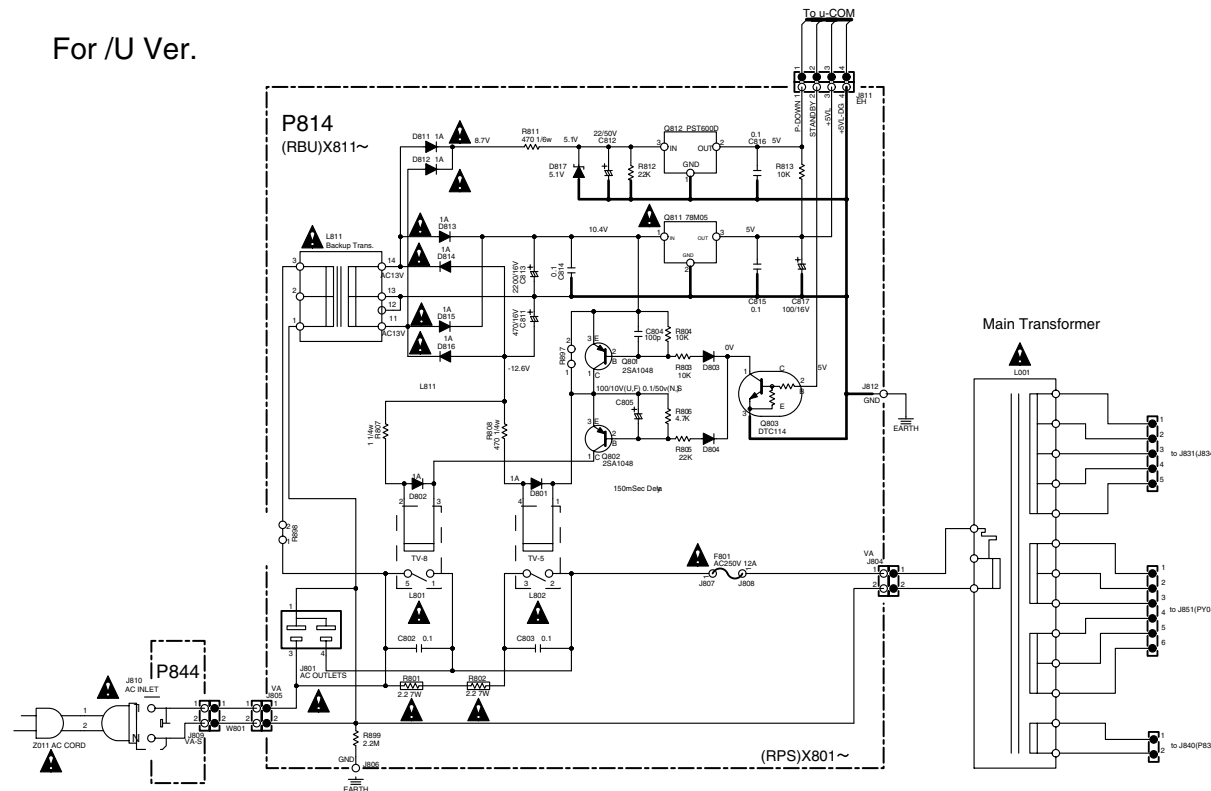
For /N/S Ver.



For /F Ver.

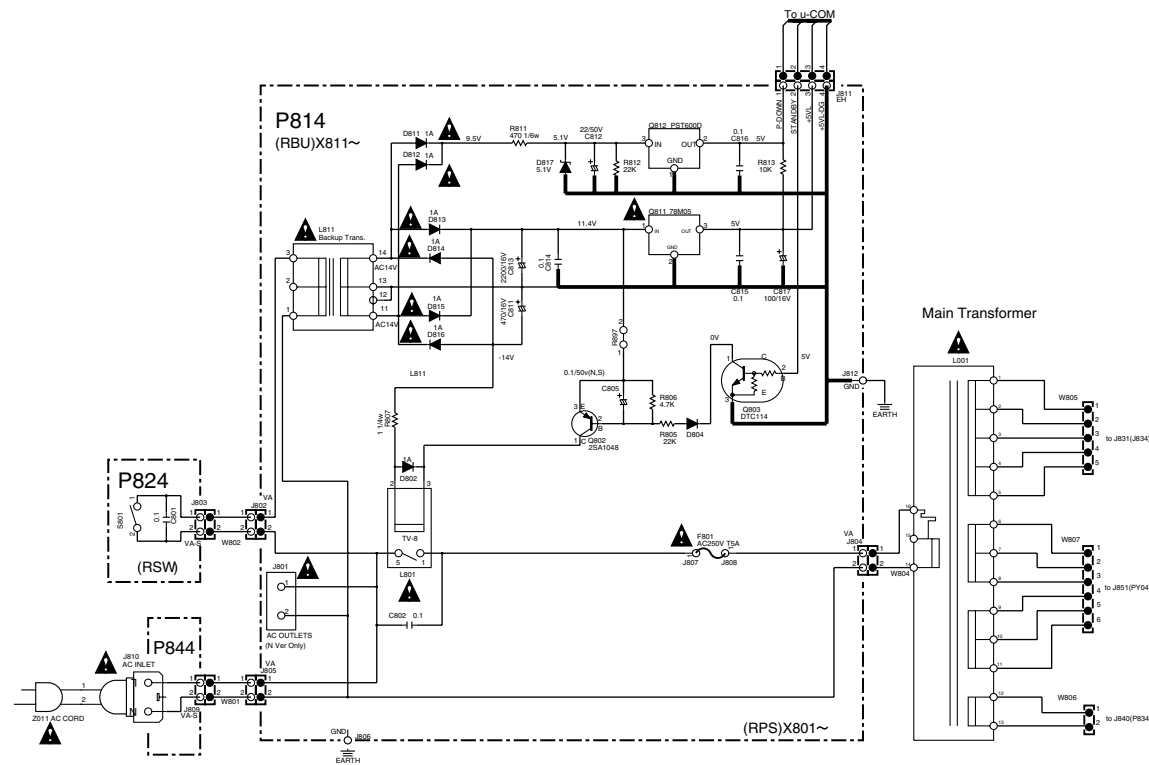


For /U Ver.

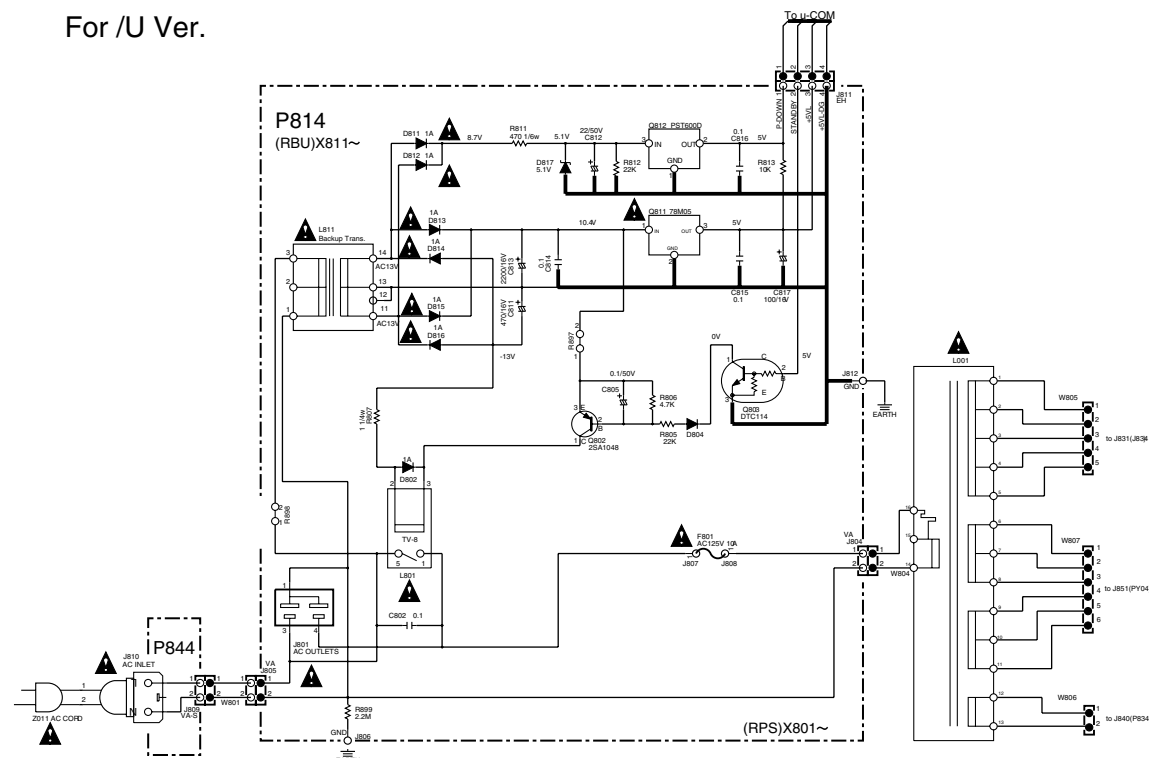


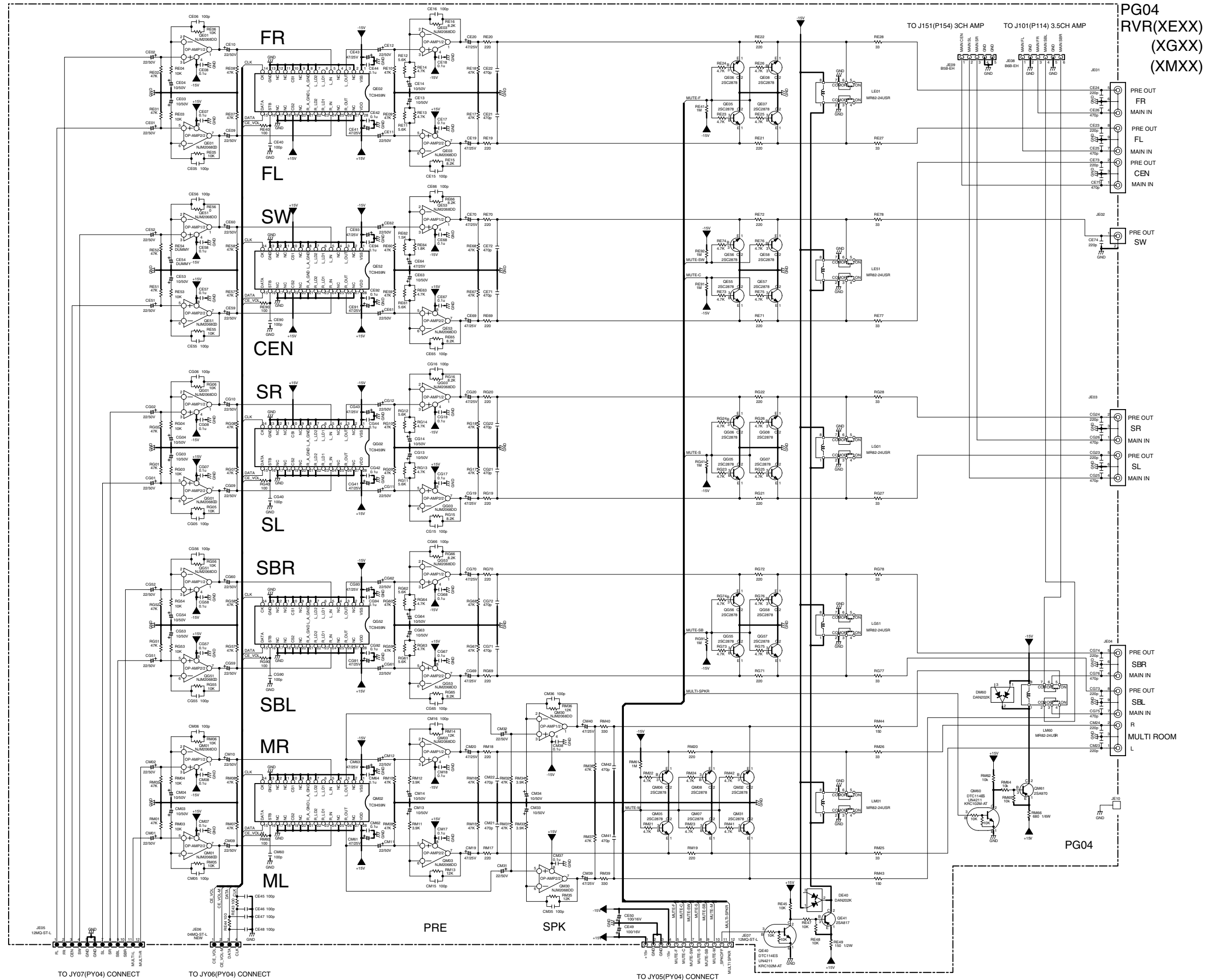
SR8200

For /N/S Ver.



For /U Ver.





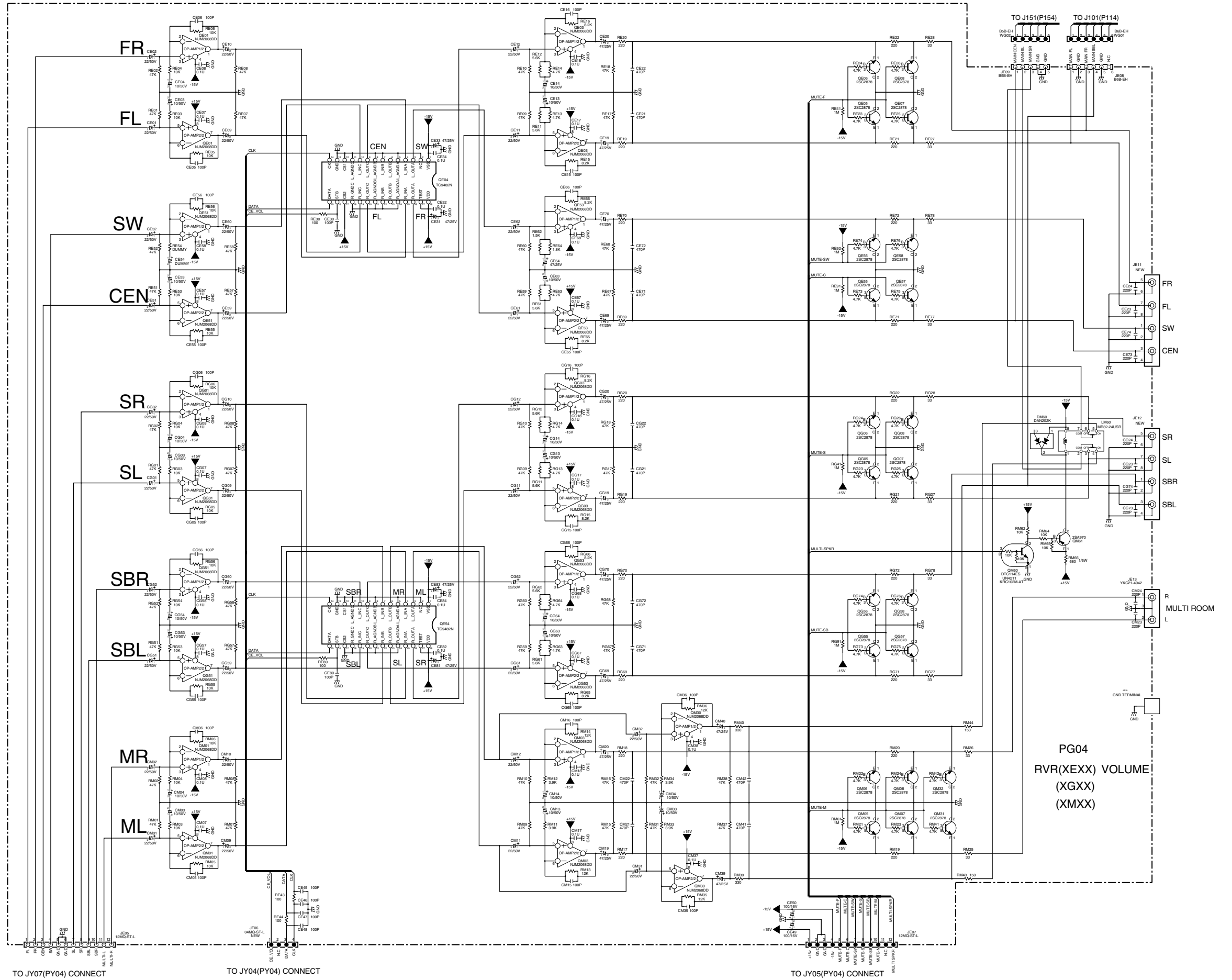
PG04
RVR(XEXX)
(XGXX)
(XMXX)

PRE OUT
FR
MAIN IN
PRE OUT
FL
MAIN IN
PRE OUT
CEN
MAIN IN

PRE OUT
SW

PRE OUT
SR
MAIN IN
PRE OUT
SL
MAIN IN

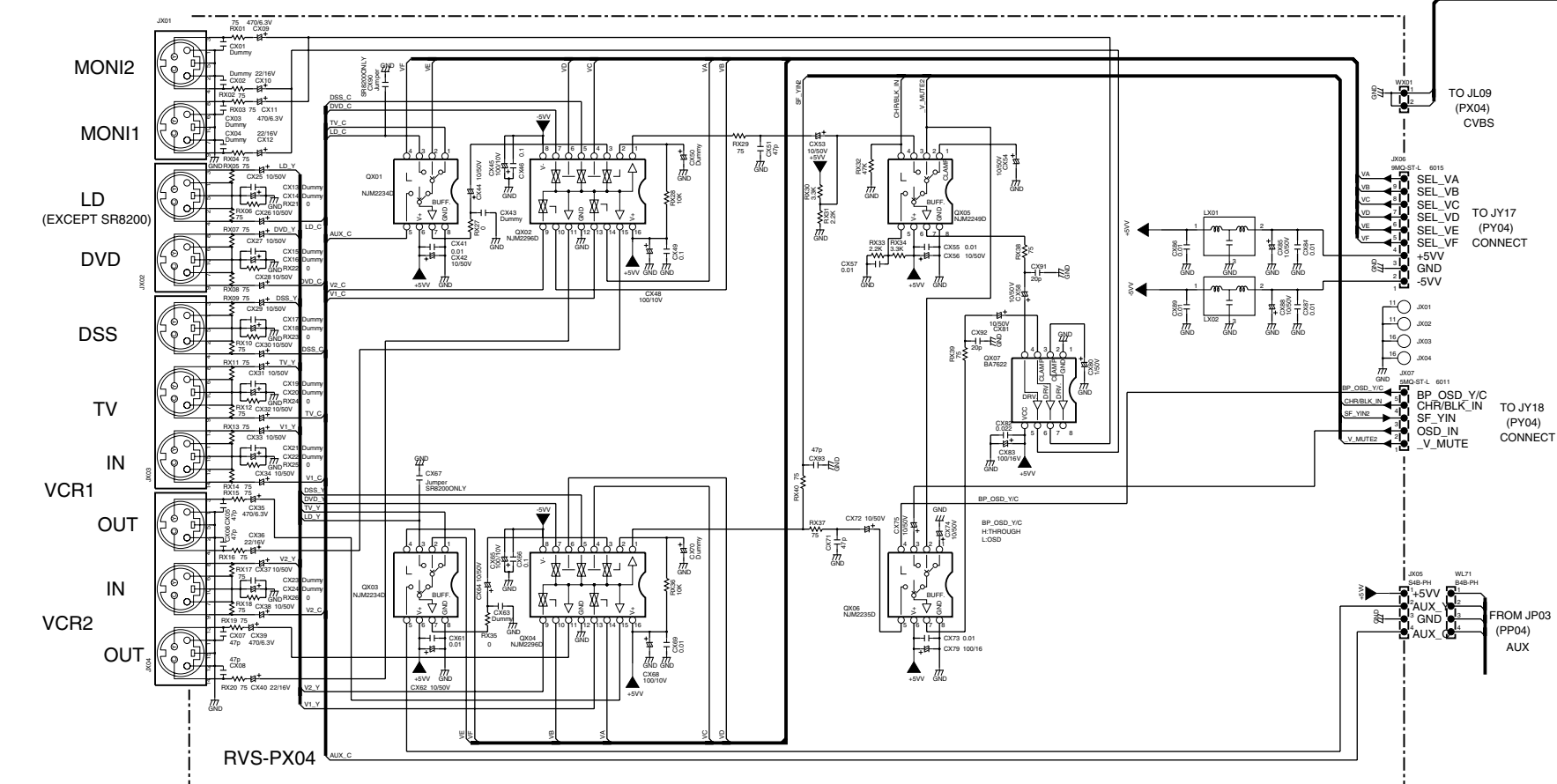
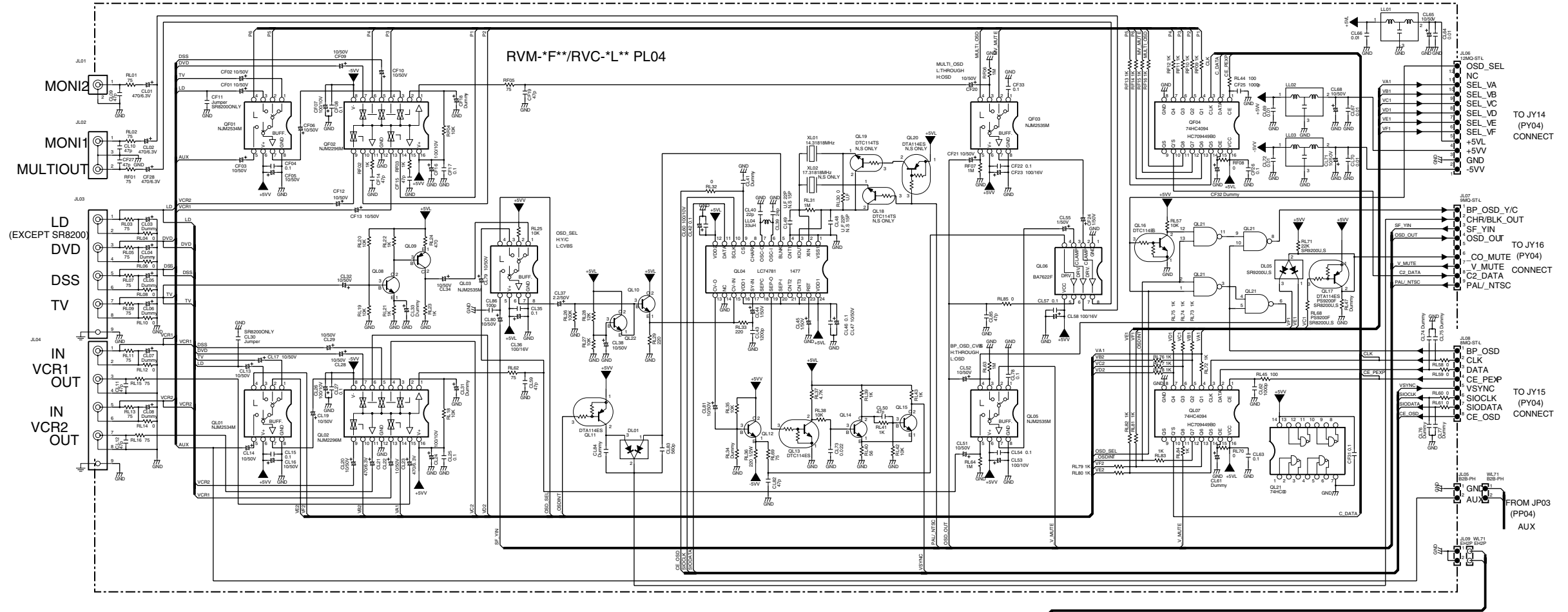
PRE OUT
SBR
MAIN IN
PRE OUT
SBL
MAIN IN
R
MULTI ROOM
L



TO JY07(PY04) CONNECT

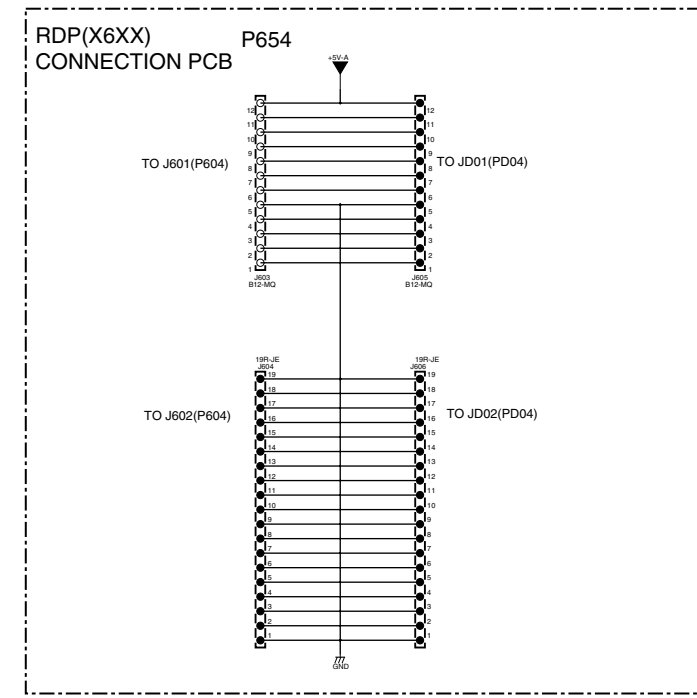
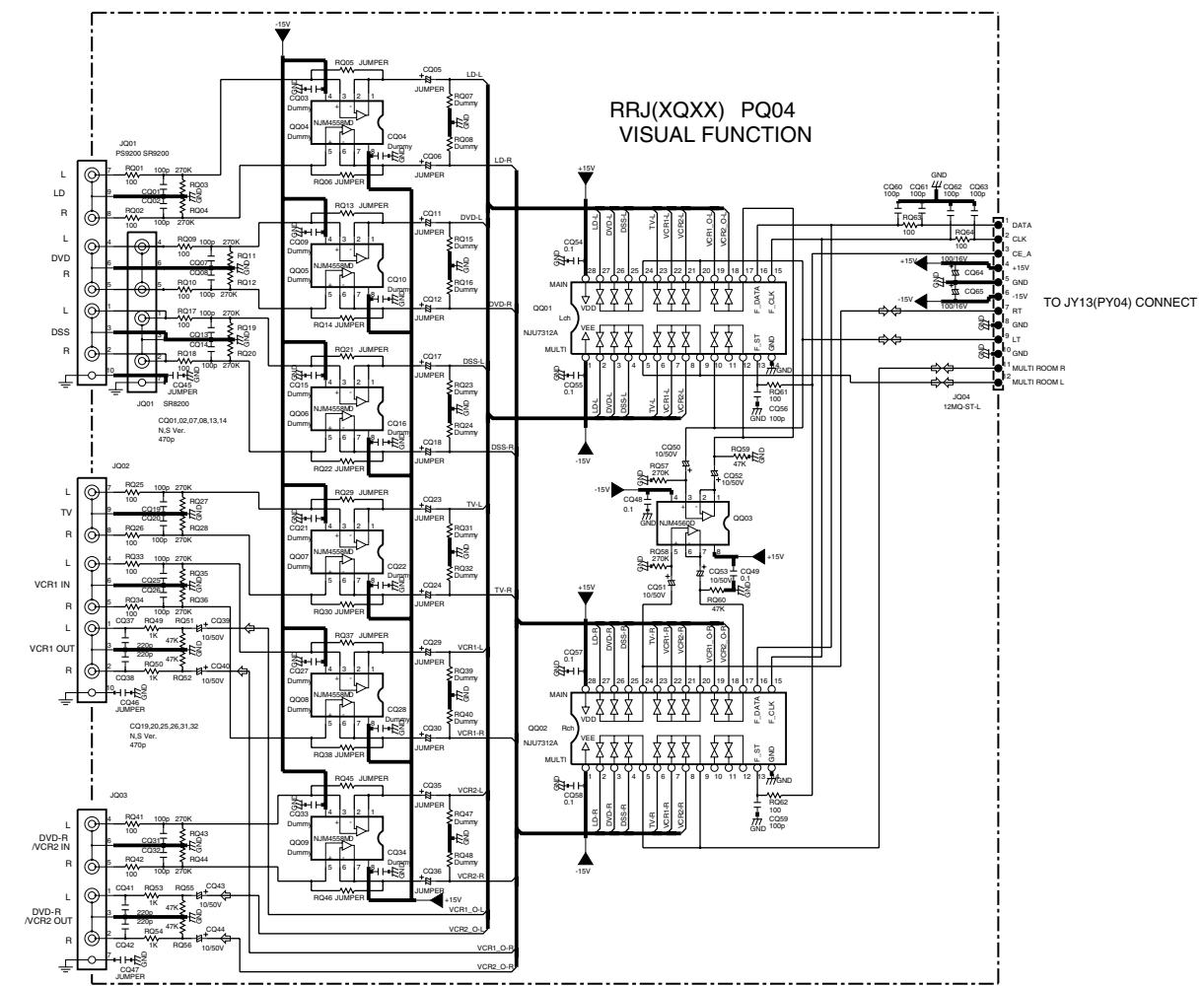
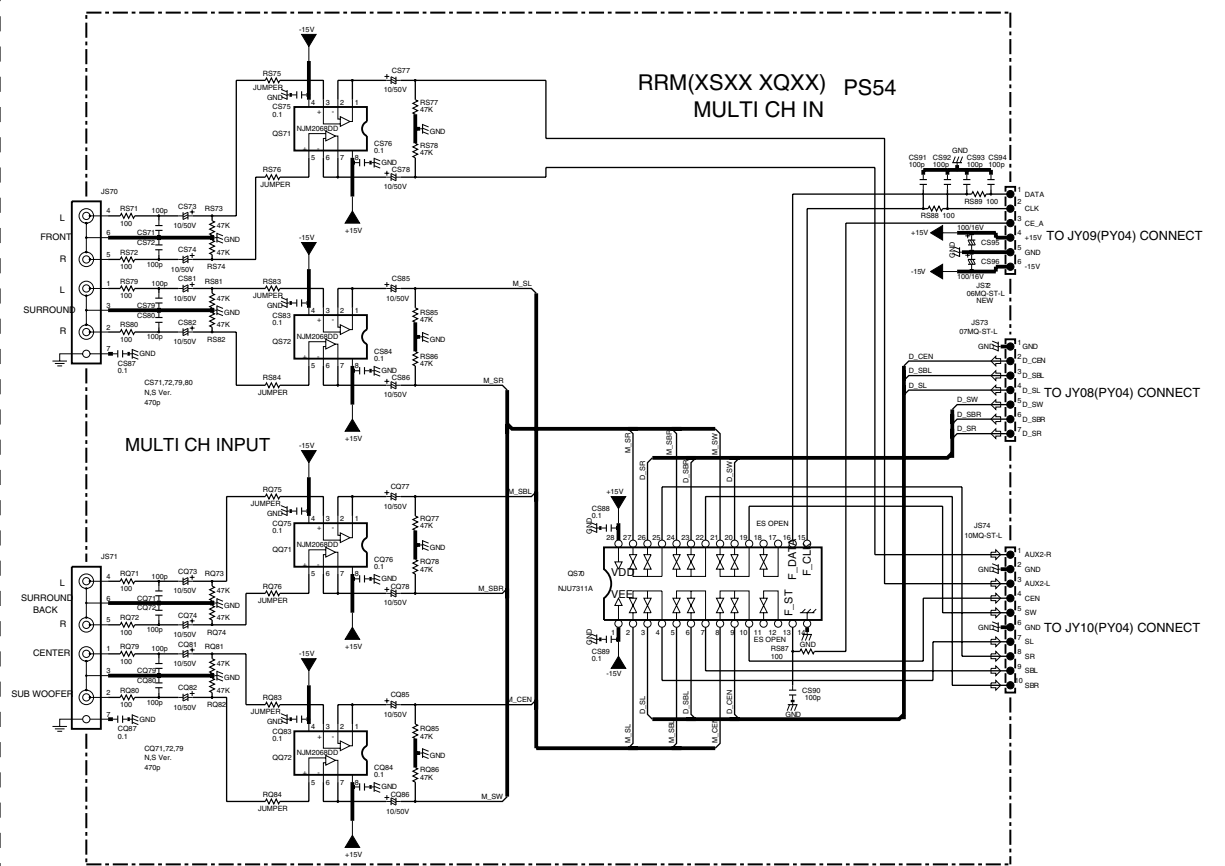
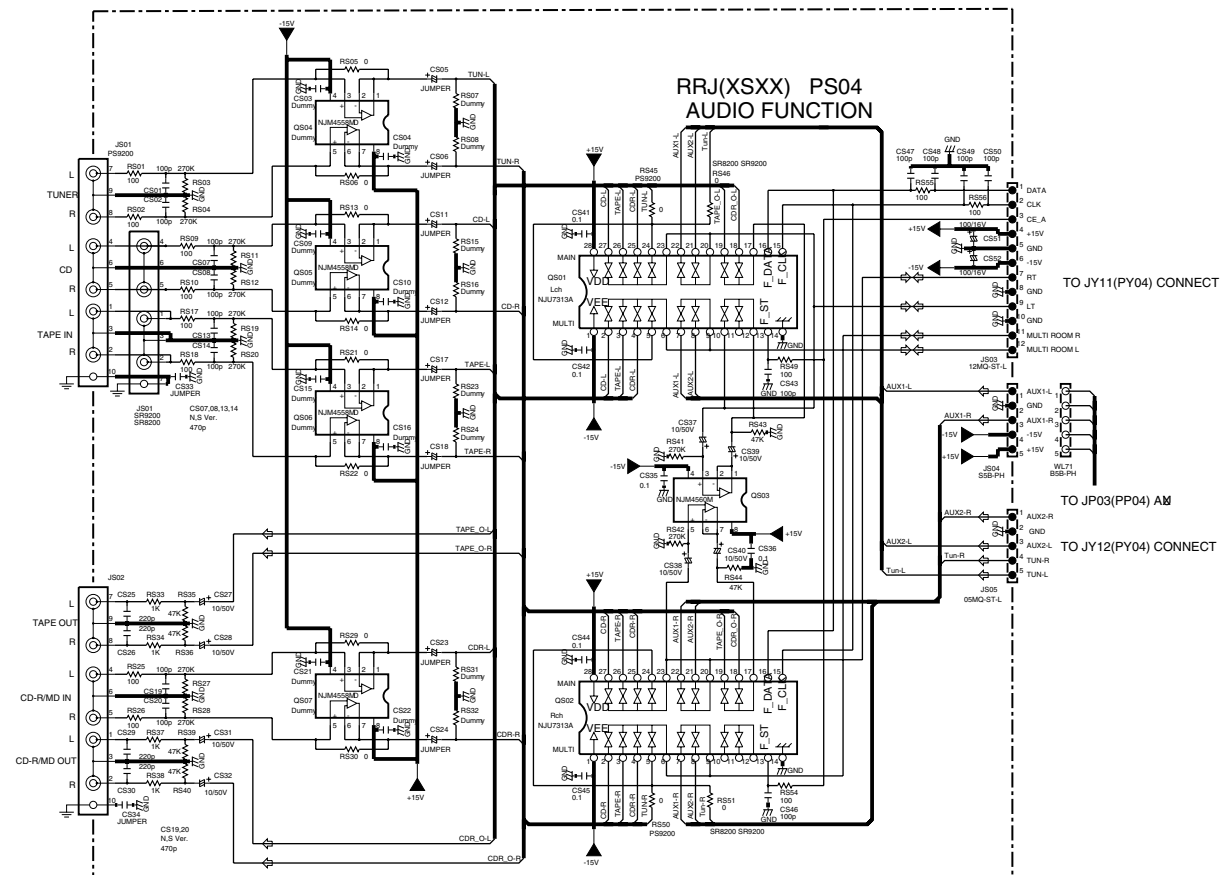
TO JY04(PY04) CONNECT

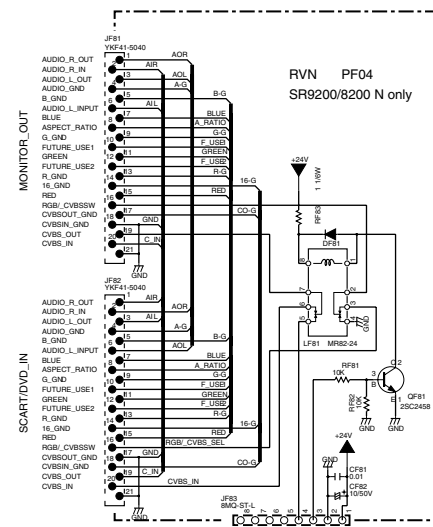
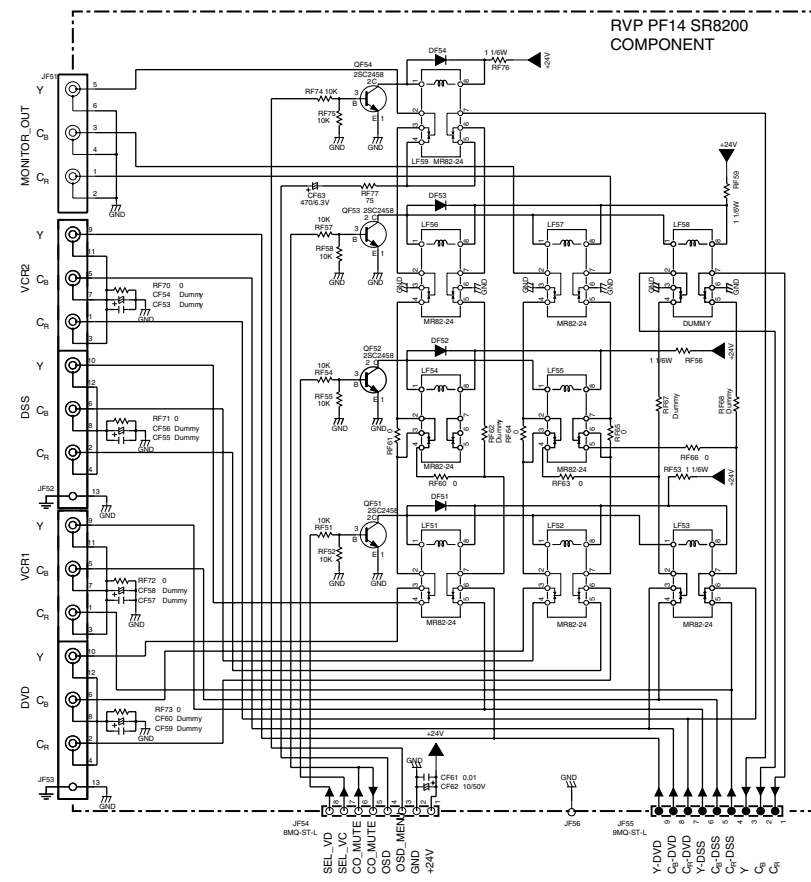
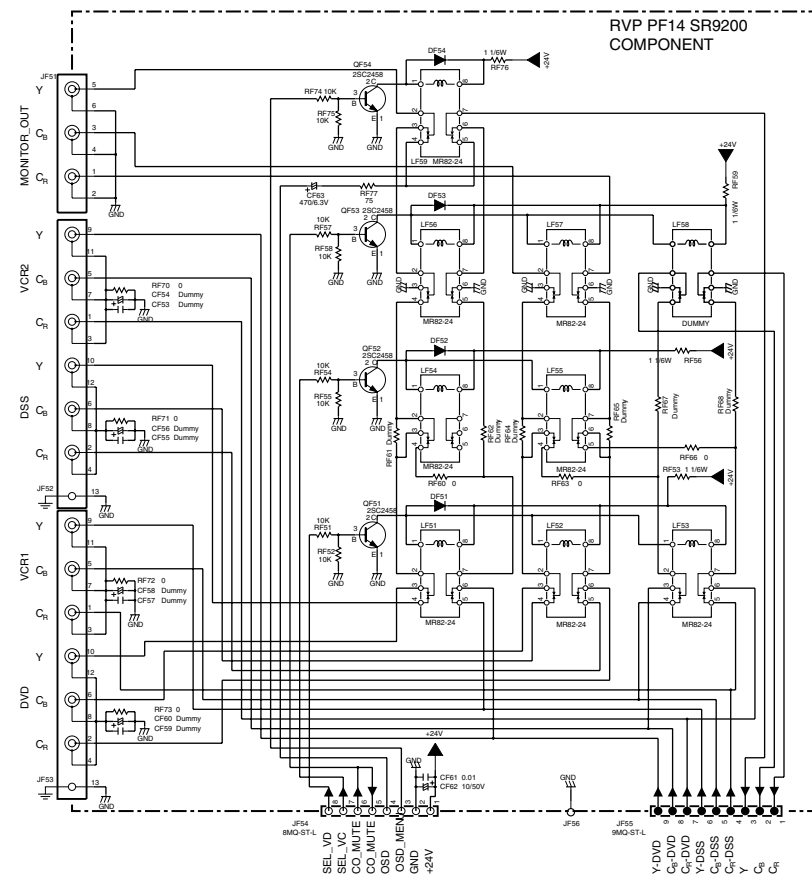
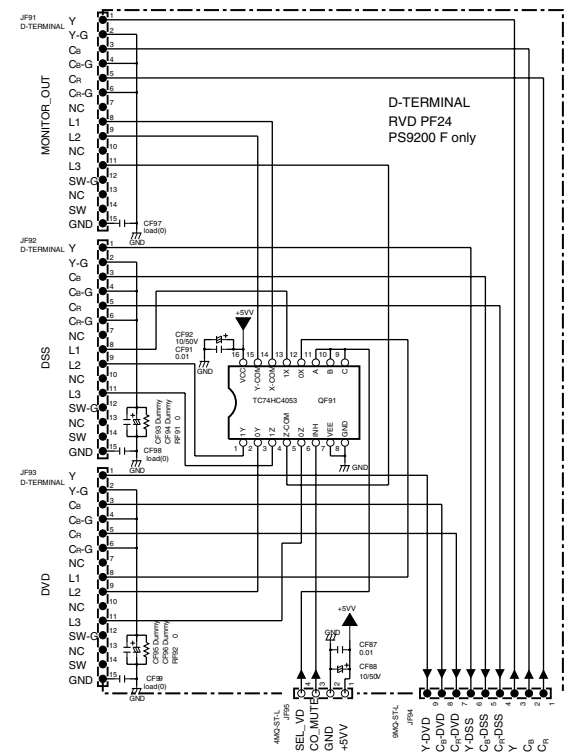
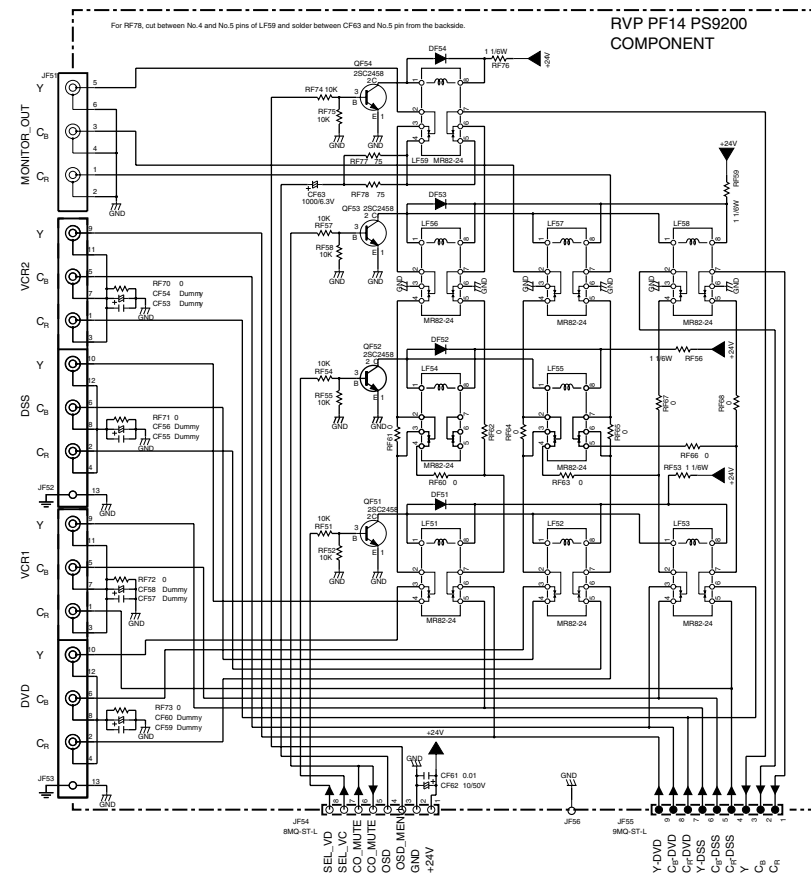
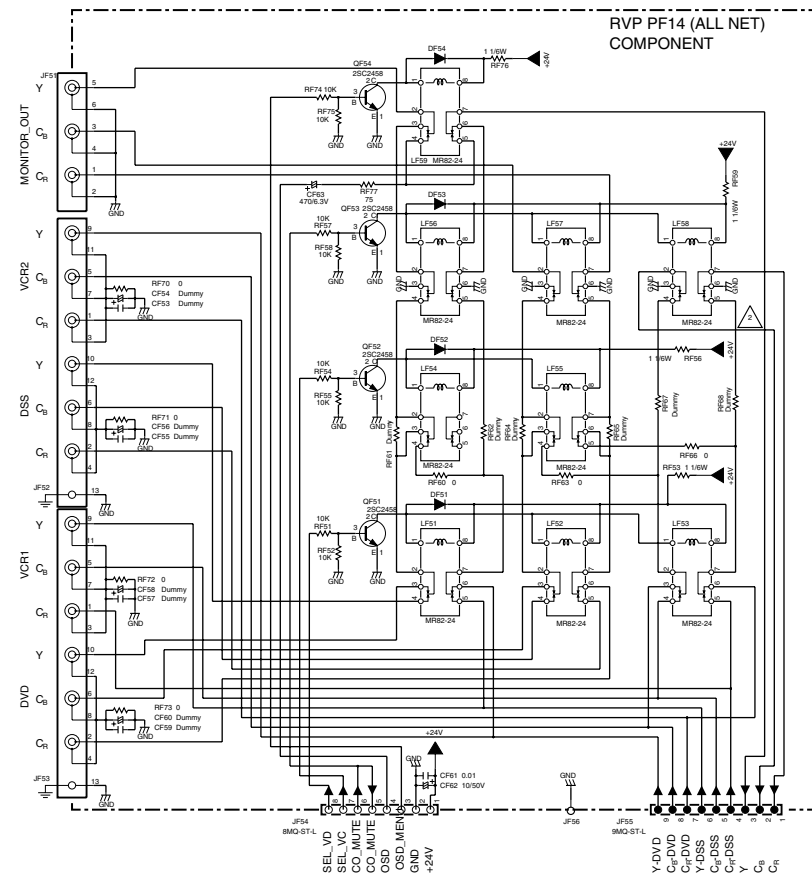
TO JY05(PY04) CONNECT



MAIN ROOM CONTROL							MULTI ROOM CONTROL						
	VA	VB	VC	VD	VE	VF		VA	VB	VC	VD	VE	VF
TV	H	H	H	H	L	L	TV	H	H	H	H	L	L
DVD	H	H	L	L	H	H	DVD	H	H	L	L	*	*
LD	H	H	H	H	H	L	LD	H	H	H	H	H	L
VCR1	L	H	H	H	H	H	VCR1	L	L	L	L	*	*
VCR2	H	L	H	L	H	H	VCR2	H	L	L	L	*	*
DSS	H	H	L	H	H	H	DSS	H	H	L	H	*	*
AUX	H	H	H	H	L	H	AUX	H	H	H	H	H	H

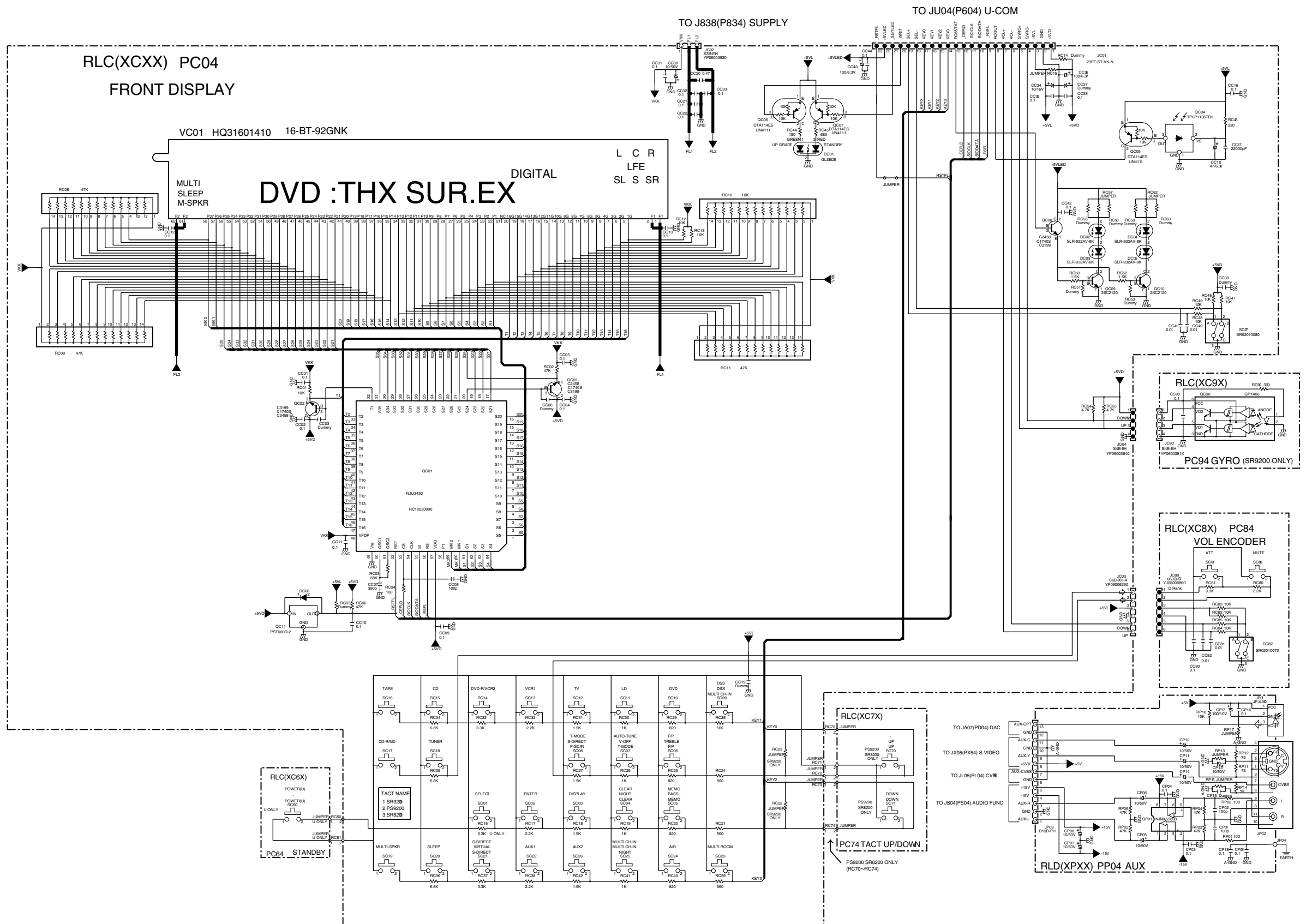
*DONT CARE

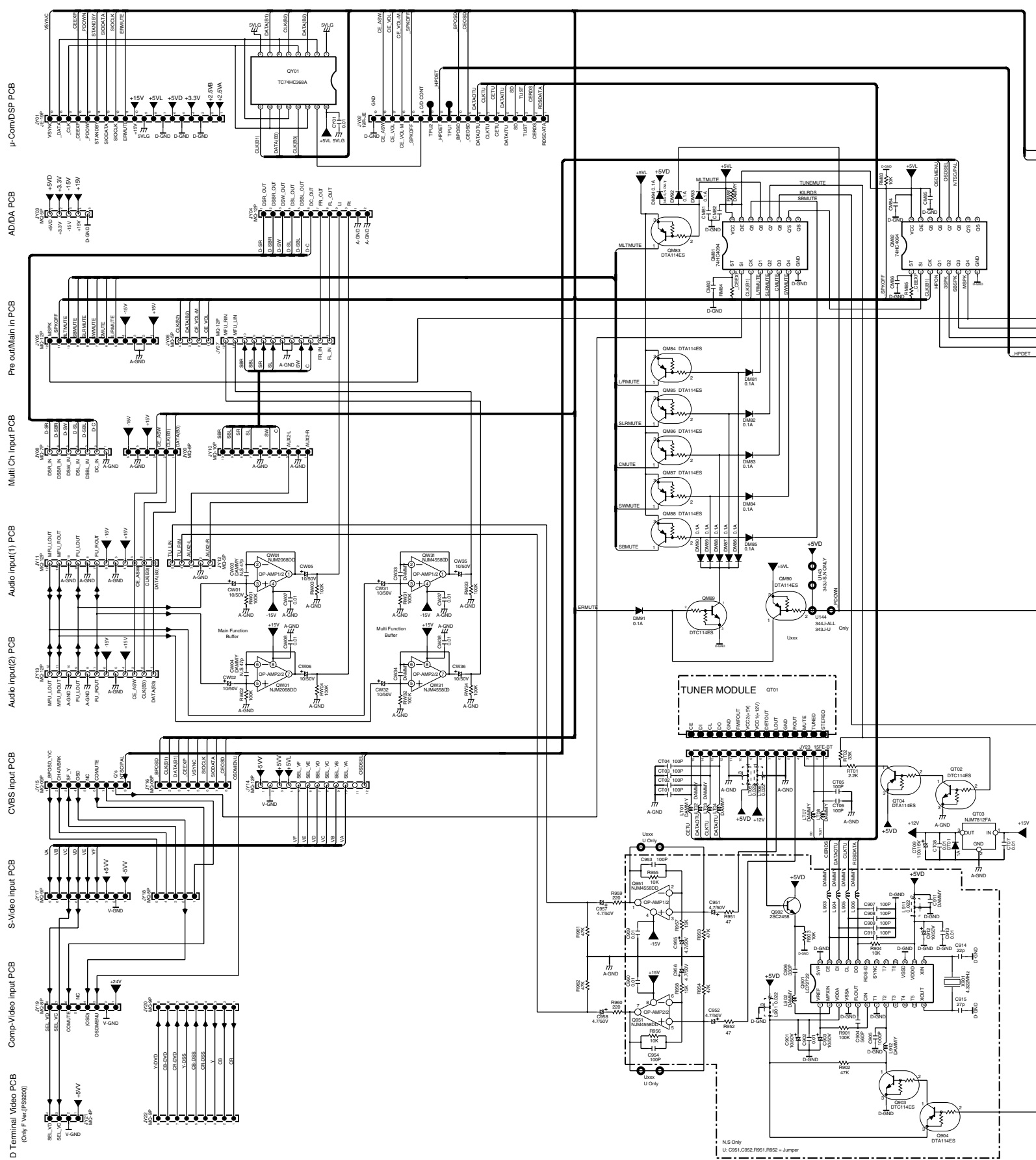




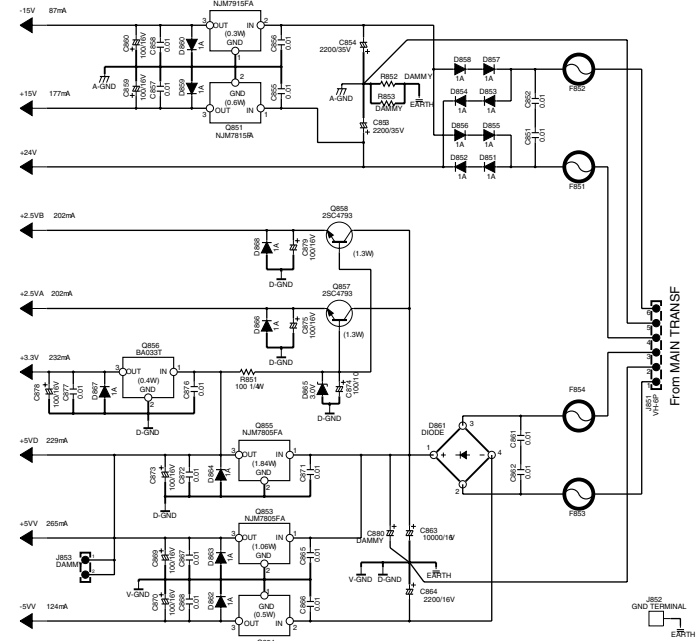
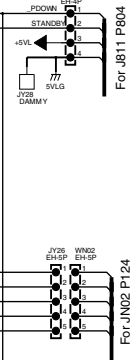
COMPONENT CONTROL

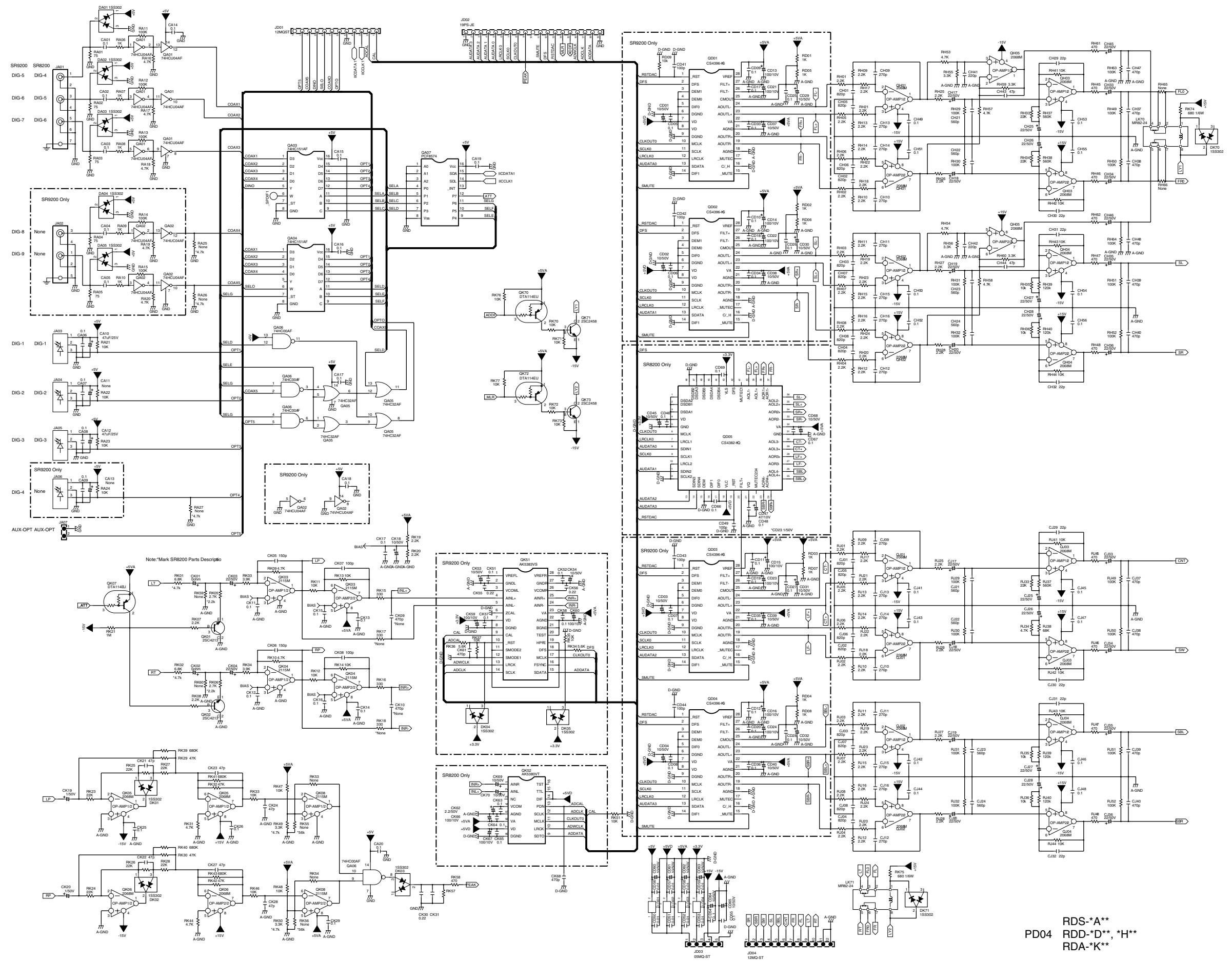
	VC	VD
DVD	L	L
VCR1	H	H
VCR2	H	L
DSS	L	H

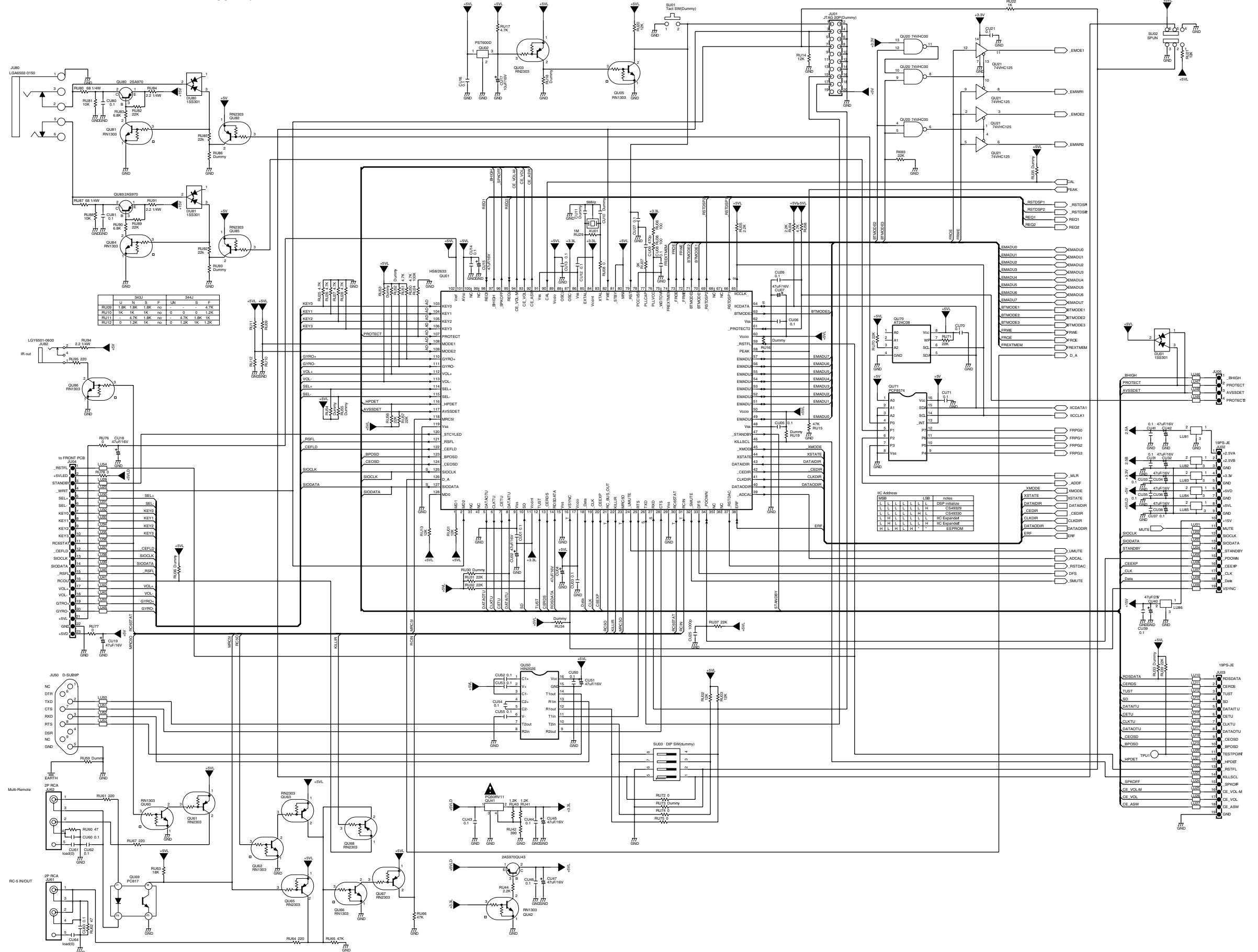




PY04
 RCN-*Y**/RVR-*M,W**/RTU-*T**
 RTR-*9**/RPS-*8**







U	N	F	LN	S	F
RL03	1.8K	1.8K	no	0	4.7K
RL10	1K	1K	no	0	1.2K
RL11	4.7K	1.8K	no	0	4.7K 1.8K 1K
RL12	0	1.2K	1K	no	0 1.2K 1K 1.2K

IC Address	MSB	LSB	Notes
L L L L L L L L L L	L	L	EEPROM
L L L L L L L L L L	L	L	EEPROM
L L L L L L L L L L	L	L	IC Expansion
L L L L L L L L L L	L	L	IC Expansion
L L L L L L L L L L	L	L	EEPROM